Characterization and Modeling of the Substrate Noise and Its Impact on the Phase Noise of VCO

Huailin Liao, Subhash C. Rustagi, Jinglin Shi, Yong Zhong Xiong

Institute of Microelectronics, 11 Science Park II, Science Park, Singapore,117685

Abstract – This paper presents a simple scheme for estimating the digital switching noise at the sensitive RF nodes with the help of a lumped element model for the substrate network. The model parameters have been extracted from the 2-port RF measurements. The efficacy of different isolation schemes such as grounded P+ guard bars and deep N-well has been investigated using phase noise of a VCO as a figure of merit.

I. INTRODUCTION

With the scaling of the CMOS technology into the deep sub-micron regime, it has become feasible to realize single chip transceivers with reduced cost and increased functionality. Integration of digital base band and RF front ends, however, makes the RF blocks vulnerable to the coupling of the digital switching noise through the common substrate bringing the investigations of substrate coupling noise into the forefront. Digital switching noise, thus, should be factored into the designs in the beginning. A number of authors have presented their own routine to model substrate noise [1],[2]. In this paper, we present a simple lumped element network model of the substrate for representing the noise coupling. The model elements are extracted from the 2-port RF measurements up to 10GHz. Digital switching noise coupled into the substrate is measured using an on-chip digital noise emulator circuit for the digital noise injection and a P+ diffusion into the P-substrate as the sensing element. Measured data is interpreted with the help of circuit simulation using the extracted substrate network. A simple scheme is suggested for estimation of the digital switching noise coupling through the substrate into sensitive RF nodes. Further, the efficacy of different isolation schemes such as P+ guard bars and deep N-well etc. is investigated using the phase noise of a Voltage Controlled Oscillator (VCO) as the figure of merit.

The test structures used in this study are described in section-II. Section-III describes the lumped element substrate network model and its extraction from the RF measurements. The measurement of substrate noise injected in the substrate from the digital switching noise emulator is reported along with a simple scheme for estimation of switching noise at the sensitive nodes. The evaluation of the effect of substrate noise on the phase noise of a VCO with and without different isolation scheme is described in section V. Section VI summarizes the main conclusions.

II. TEST CHIP

A standard 0.18um CMOS n-well process with single level poly-silicon and six metal levels and an optional deep N-well was chosen for these investigations. The test structures put on the test chip included a set of 2-port substrate modeling designs schematically shown in Fig. 1 where port 1 is connected to different types of noise injectors such as P+ diffusion, P+ diffusion in deep N-well, P+ diffusion with P+ grounded guard bar, N+ diffusion, with and without P+ guard bar and deep N-well etc. A digital switching noise emulator test structure comprising a ring oscillator with 5 stages of inverter buffers driving large capacitive loads formed by the junction capacitors at the drain nodes of NMOS transistors and a P+ substrate tap for measuring the digital switching noise were included. The VCO test structure consisted of a pair of cross-coupled CMOS transistors and a symmetric inductor. The circuit schematic of the VCO is shown in Fig. 2 There also was put a provision of protecting both the digital noise emulator as well as the VCO to be isolated by deep N-well and grounded guard bars. Fig. 3 shows the photomicrograph of the test chip.

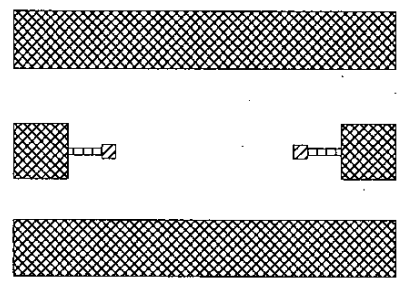

Fig.1 The layout of basic test structure for characterizing substsrate network.

0-7803-7694-3/03/$17.00 © 2003 IEEE

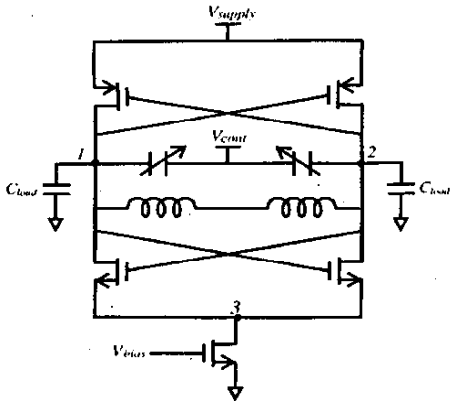

Fig.2. The simplified schematics of negative resistance VCO for a WLAN tranceiver

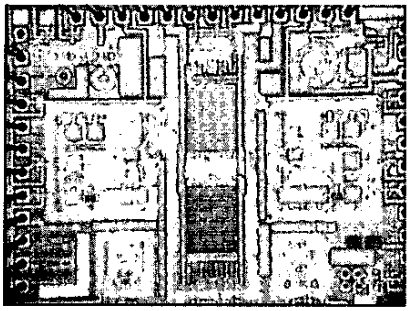

Fig.3 The micrograph of test chip

III. EXTRACTION OF THE SUBSTRATE NETWORK MODEL

Network in the dotted enclosure in Fig.4.was chosen to model the substrate in this study [3],[4]. The measurements up to 10GHz showed that a simple resistive network is not sufficient to represent the substrate and complex admittances are essential. The model parameters (network elements) of the pi-network were extracted for different types of noise injectors described above using 2-port RF measurements with the help of an HP8510C network analyzer. Fig. 5 shows the variation of the extracted network parameters with the distance of the noise source from the noise injector. It is easily observed that the model parameters scale with the distance between the noise source and the noise sensor.

The variation of the isolation parameter S21 as a function of frequency for different types of noise sources is shown

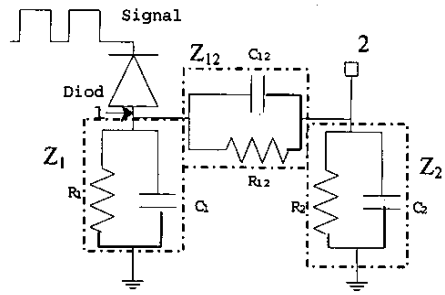

Fig.4 The layout of basic test structure for substrate isolation measurement

in Fig. 6. It is interesting to observe that the magnitude of S21 remains almost constant with frequency when the noise injector is either a P+ diffusion or P+ diffusion with a P+ grounded guard bar. This fact will be made use of in developing a scheme for estimation of digital noise in the next section.

IV. ESTIMATION OF THE DIGITAL NOISE INJECTED INTO THE SUBSTRATE

With the help of the network in Fig.4 the s-domain volatge at node 1 when a pulse of rise-time τ_p with amplitude V_{dd} is applied at the input can be written as:

$$V_1(s) = \frac{sC_{diode}V_{dd}Z1}{(1+\tau_p s)} \quad (1)$$

It is assumed that Z12 in Fig. 4 is much larger compared to Z1 to arrive at equation (1). C_{diode} represents the capacitance of the N+ diffusion in the substrate for the N+ noise injectors such as N+ drain nodes of the NMOS transistors in the noise emulator. Interestingly, one may observe from eqn. (1) that $V_1(s)$ is proportional to Z1 implying that good grounding of the substrate should help in suppressing the injected noise. Further, as the noise travels through the linear substrate network of Fig. 4, the noise voltages at nodes 2 and 1 can be related in frequency domain as follows:

$$V2(f) = A(f)V1(f) \quad (2)$$

Where A(f) represents the voltage attenuation. As described above, the measurements for the P+ noise injector indicates that S21 remains constant as a function of frequency, therefore, it will be reasonable to assume that A(f) is constant with frequency. Eqn. (2) can then be re-written for any distance d between the noise injection and sensing point as

$$V2(f) = |A|\, V1\exp(j2\pi f \cdot \xi(d)) \quad (3)$$

Where $\xi(d)$ gives the phase shift as a function of the distance. From equation (3), the time domain relationship between V1 and V2 can be written as:

$$V2(t) = |A|V1(t - \xi(d)) \quad (4)$$

Significance of eqn. (4) is that the noise at any sensitive node due to noise injectors can be very efficiently

estimated with the help of simple shift and multiply operation.

We measured the noise injected into the substrate by the digital switching noise emulator by a spectrum analyzer (R&S) using a P+ substrate tap. Fig. 7 shows the measured spectrum. The noise at the substrate node was also simulated using the extracted substrate network with ADS (Agilent Technologies) simulator. The simulated spectrum is shown in Fig. 8. The similarity in noise power levels between Fig. 7 and Fig. 8 demonstrates the efficacy of the extracted substrate network and hence the noise estimation scheme discussed above. We wish to point out here that the lower noise power levels in the measured spectrum are invisible due to the noise floor of the spectrum analyzer setup used in these measurements.

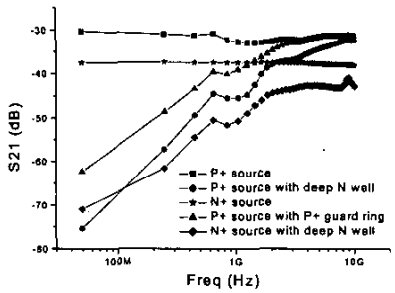

Fig.6 Measured S_{21} for different noise sources.

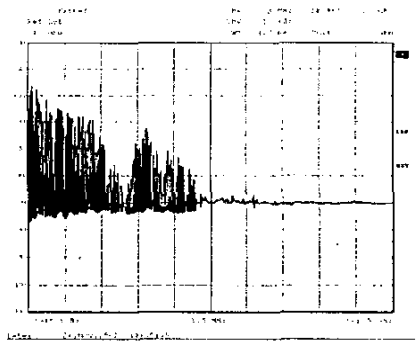

Fig.7 The substrate noise spectrum at P+ DIF sensor output

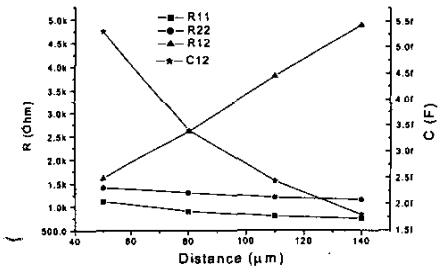

Fig.5 Extracted parameters for P+ DIF source.

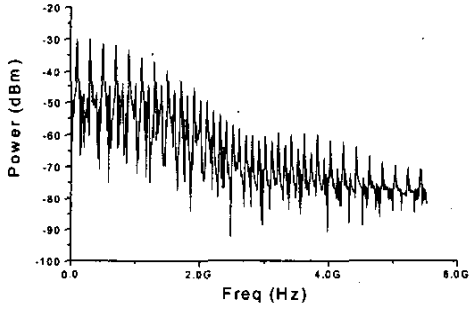

Fig.8 Simulated substrate noise spectrum.

V. EFFECT OF THE INJECTED SUBSTRATE NOISE ON THE PHASE NOISE OF A VCO

Fig. 9(a) and (b) show the output spectrum of the VCO when the digital switching noise emulator is "on" and "off" respectively. The center frequebcy of the VCO is 3.5GHz and the power levels are –18 dBm. When digital emulator is switched on, there are a lot small harmonics around the center frequency of the VCO. Fig. 10(a) and (b) show the measured phase noise of the VCO when the digital emulator and VCO are protected by different isolation schemes respectively. In order to avoid the noise from the DC supply to contaminate the measured data, the battery was used for the voltage supply.

It is observed from Figs. (9) and (10) that when the digital noise emulator is switched on without any protection, the phase noise of the VCO degrades by about 12dBc per hertz. The effect of different noise suppression schemes as applied to the digital noise emulator on the phase noise is shown in Fig. 10(a) while Fig. 10(b) shows the same for the same noise suppression schemes isolating the VCO. It can be concluded that the deep N-well almost completely

isolates the substrate noise. The grounded P+ guard bars are a little less effective. This could be on account of inductance of the bond wire or otherwise which affects the level of grounding. Careful grounding of the guard bars may need more investigations.

VI.CONCLUSION

A simple scaleable model for the substrate network has been presented in this paper along with the extraction of the model parameters from the 2-port RF measurements. A simple scheme to estimate the digital switching noise coupling into the sensitive substrate nodes has been proposed. The extracted substrate network has been shown to be a potentially efficient tool in the estimation of substrate coupling noise. The phase noise of a VCO has been used as a figure of merit to evaluate different protection schemes such as P+ ground bars, deep N-Well and their combination. It is observed that deep N-well comes out as the most effective isolator for the substrate coupling noise.

REFERENCES

[1] Min Xu, David K. Su,Derek K. Shaeffer, Thomas H. Lee, Bruce A. Woole,, "Measuring and Modeling the Effects of Substrate Noise on the LNA for a CMOS GPS Receiver," *IEEE Journal of Solid-States Circuits Vol. 36, No. 3, March 2001 pp. 473-485.*

[2] Ranjit Gharpurey and Robert G.Meyer, "Modeling and analysis of substrate coupling in integrated circuits", *IEEE Journal of Solid-State circuits, Vol. 31, No. 3, March 1996, pp.344-353.*

[3] W. Jin Y. Eo, J.I. Shim, W.R.Eisenstadt, M.Y.park and H.Y.Yu, " Silicon substrate noise modeling , analysis and experimental verification for Mixed Signal integrate circuits design.," *2001 IEEE MTT-S digest, pp.1727-1731.*

[4] Martin Pfost, and Hans-Martin Rein, " Modeling and Measurement of Substrate Coupling in Si-Bipolar IC's up to 40 GHz " *IEEE Journal of Solid-States Circuits, Vol. 33, No. 4, April 1998, pp.582-591.*

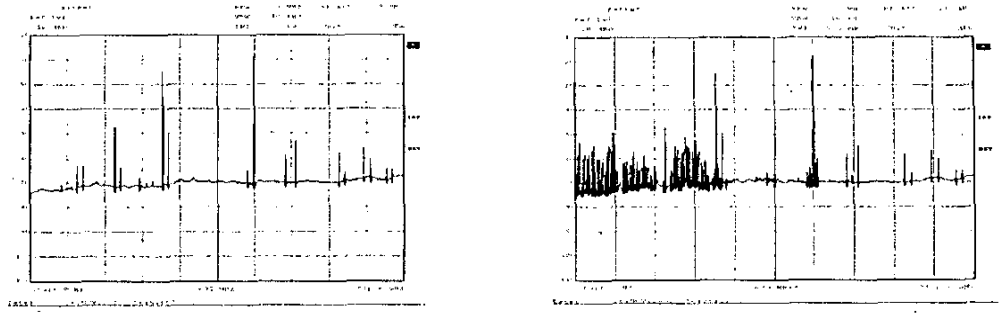

Fig.9 (a) and (b) Output spectrum of VCO when digital emulator is off and on

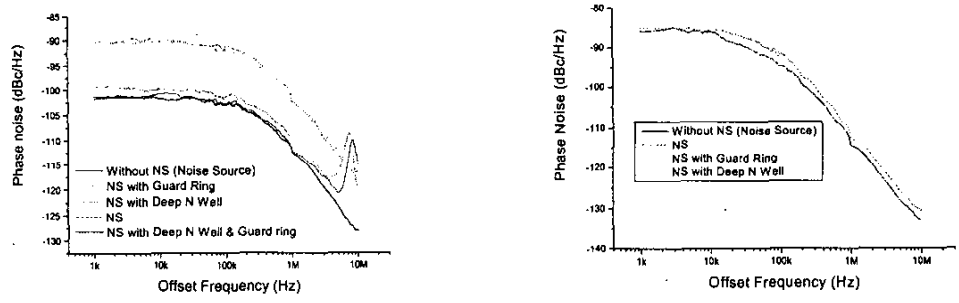

Fig.10 (a) and (b) The comprison of phase noise when VCO and digital emulator at different coupling isolation schemes